Novel GaN Device Gate Drive Technique for High Efficiency and Noise Reduction

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Recently, high-speed switching circuits using GaN GIT have attracted attention for higher power density. In particular, GaN GIT devices have an ultrafast speed capability but tend to cause false turn-ons due to a lower threshold voltage. A simple RC-type gate drive method is usually used to prevent the false turn-on phenomenon. However, during the turn-off period, the spike gate voltage will exceed the rated voltage, it is necessary to slow down the turn-off switching speed, and the high-speed switching characteristics of GaN GIT could not be fully utilized. To solve this problem, we propose a novel GaN GIT gate drive technique using a two-step turn-off method. It is possible to simultaneously satisfy the conflicting performance of low spike voltage and high speed turn-off switching. This circuit was implemented on the board using the GaN GIT device and applied to a synchronous rectification type boost converter. It is confirmed experimentally that this drive technique is verified as useful.

1. Introduction

In recent years, wide gap semiconductors have attracted attention as the material for new semiconductor devices in place of silicon (Si) toward the realization of higher power density and higher efficiency of power converters[1]. The power converter is mostly occupied by cooling parts (heat sink) and passive parts (capacitor and reactor), and higher efficiency and higher frequency can realize size and cost reductions of these parts. The power converter (power conditioner, multipurpose power supply, and servo drive) as one of the product groups of OMRON is for power of several hundred W to several kW, and especially we study the application of gallium nitride (GaN) as shown in Fig. 1. The Si device has the large input and output capacitance and the poor reverse recovery operation of a body diode, while the GaN device has capacitance far lower than the former and is excellent in the reverse recovery characteristic. Therefore, the use of the GaN device can realize higher efficiency. In order to derive the material characteristic of the GaN device to the limit, the GaN devices with various internal structures, such as the vertical structure[2] and the horizontal structure[3] have been developed. The depression mode[4] GaN is a normally-on device, and the enhancement mode (E-M)[5] GaN realizes an easily handled, normally-off device. In addition, the hybrid mode (H-M)[6] structure using MOSFET has been also developed. Table 1 shows the comparison of parameters of available typical devices. Here blue and red letters show the advantages and disadvantages, respectively. GaN GIT (gate injection transistor)[7] attracts attention as a device of which normally-off action and capacitance C and electric charge Q are low as shown in Table 1 and which can realize high speed drives.

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This paper explains focusing on GaN GIT. The threshold voltage V_{th} of this device is far lower than that of the Si device as shown in Table 1, and it is very important to maintain the off state for GaN GIT. GaN GIT is sensitive to noise, and negative gate voltage is required for the prevention of the incorrect turn-on of GaN GIT by the miller current. When incorrect turn-on occurred because of the absence of negative gate voltage, the arm short-circuit phenomenon may occur, leading to catastrophic failure. The negative gate voltage is normally implemented by the bipolar power supply. In order to derive the switching performance of GaN GIT, the RC type gate drive method[8,9,10,11] proposed. Since this method can drive the gate of GaN GIT in higher voltage, high speed switching can be realized. However, the high-speed property of the turn-off generates high negative spike gate voltage.

In order to solve these problems, we propose the GaN GIT gate drive method of two-step turn-off that can simultaneously realize the contrary performance of low noise and a high-speed turn-off switching. Chapters 2 and 3 will explain the operation principle of the conventional gate drive circuit and the proposed gate drive circuit. Chapter 4 applied the proposed gate drive circuit to the synchronous rectification type DC/DC converter to verify the effectiveness experimentally.

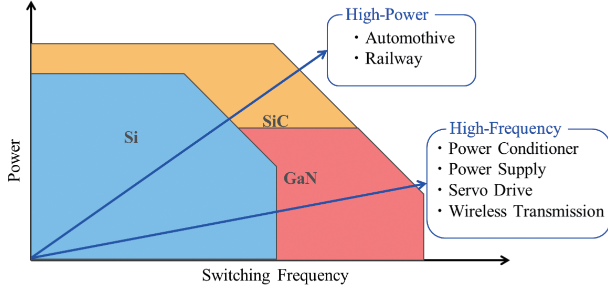


Fig. 1 Power device and application

Table 1 Comparison of device parameters

	Si	SiC	GaN H-M	GaN E-M	GaN GIT
V_{ds} [V]	600	650	650	650	600
I_d [A] Max.	35	39	34	30	31
R_{dson} [mΩ] Typ.	52	48	50	50	55
C_{iss} [pF] Typ.	2850	1118	1000	242	380
C_o (tr) [pF] Typ.	1050	194	310	160	102
Q_g [nC] Typ.	68	33	16	6.1	5.8
Q_{oss} [nC] Typ.	—	78	126	64	41
Q_{rr} [nC] Typ.	6000	125	126	0	0
V_{th} [V] Typ.	3.5	4.5	4	1.7	1.2

2. Conventional gate drive circuit

2.1 Circuit structure

Fig. 2 shows the structure of the conventional RC type gate drive circuit. Although this circuit is simple and has been actually used for many years, the high negative spike gate voltage may be caused during the higher speed turn-off as shown in Fig. 3 (part encircled by the red line). Therefore, it hinders high frequency switching.

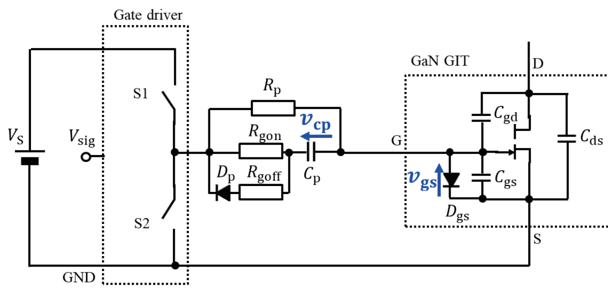


Fig. 2 Conventional gate drive circuit

2.2 Operation principle

Fig. 3 shows the operation sequence. Fig. 4 shows the equivalent circuit in each period of the conventional RC type gate drive circuit. Concerning Fig. 3, since the resistances R_{gon} and R_{goff} are very small, the operation principle will be explained neglecting these.

TERM I [$T_0 \le t \le T_1$]:

When switch S1 is turned on at T_0, the input capacitance ($C_{iss} = C_{gs} + C_{gd}$) of GaN GIT starts charging through the capacitance C_P. Simultaneously, the electric current starts to flow in the parasitic diode D_{gs} formed between the gate and the source of GaN GIT.

TERM II [$T_1 \le t \le T_2$]:

When turn-on is completed, the gate current always flows through R_P to the parasitic diode between the gate and the source to maintain the turn-on condition. v_{gs} is clamped by the forward voltage (V_F) of the parasitic diode. This depends on the band gap of GaN GIT. The gate resistance R_P is generally designed so that V_F of the parasitic diode is approximately 3.5 V. Voltages V_{gs_II} and V_{CP_II} in the period II are given by the equations (1) and (2), where V_S is the gate supply voltage.

$$V_{gs_II} = V_F \tag{1}$$

$$V_{CP_II} = V_S - V_F \tag{2}$$

TERM III [$T_2 \le t \le T_3$]:

When switch S2 is turned on at T_2, the capacitance C_{iss} starts discharging through the capacitance C_P. v_{gs} decreases corresponding to that. Negative voltage V_N can be calculated using the general MOSFET equation (3)[12], where Q_g is the total gate electric charge from 0 V to V_F. Switching speed can be adjusted by the resistance R_{goff}. Since the gate voltage sharply changes to negative, the high spike gate voltage is additionally generated in V_N.

$$V_N = \frac{Q_g - C_P \cdot V_{CP_II}}{C_{iss} + C_P} \tag{3}$$

TERM IV [$T_3 \le t \le T_4$]:

The capacitances C_{iss} and C_P are discharged through the resistance R_P. The gate voltage v_{gs} approaches 0 V in the above RC time constant. v_{gs_IV} voltage during the period IV is given by the equation (4).

$$v_{gs_IV}(t) = V_N \cdot \exp\left[\frac{-(t - T_3)}{R_P (C_P + C_{iss})}\right] \tag{4}$$

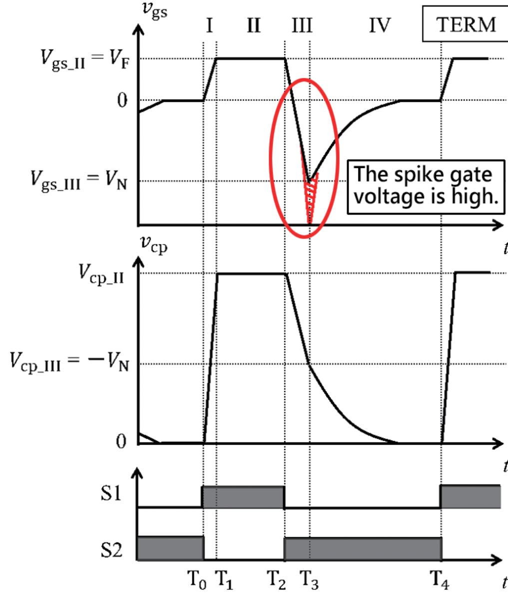


Fig. 3 Operation sequence of conventional gate drive circuit

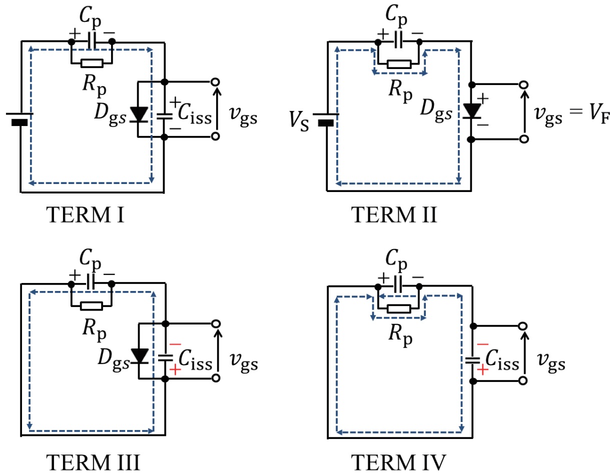


Fig. 4 Equivalent circuit of conventional gate drive circuit

3. Proposed gate drive circuit

3.1 Circuit structure

Fig. 5 shows the gate drive circuit of the two-step turn-off constituted by Q_S, R_S, and C_S (part surrounded by red dotted line). The active miller clamp MOSFET Q_S used for preventing the incorrect turn-on of a power transistor caused by the miller current is implemented in a commercialized gate driver.

When the miller clamp function is used, the gate voltage of the power transistor is generally clamped at approximately less than 2 V in the off condition. The proposed gate drive circuit can reduce the spike gate voltage during turn-off as shown in Fig. 6 (encircled in red).

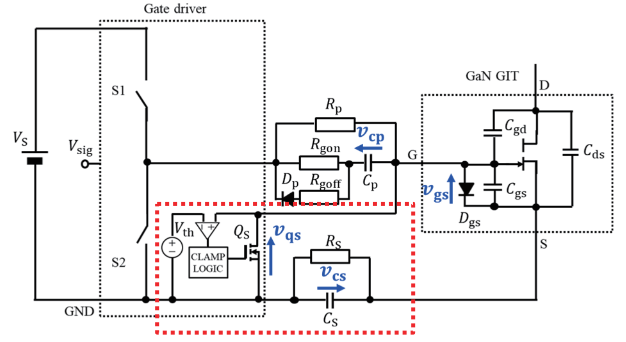


Fig. 5 Proposed gate drive circuit

3.2 Operation principle

Fig. 6 shows the operation sequence. Fig. 7 shows the equivalent circuits of the proposed gate drive circuit in each period. Concerning Fig. 7, the resistances R_{gon}, R_{goff}, and the capacitance of MOSFET Q_S are neglected because they are so small. It is assumed that the capacitance C_P is much smaller than the capacitance C_S.

TERM I [$T_0 \le t \le T_1$]:

Switch S1 is turned on at T_0, the input capacitance (C_{iss}) of GaN GIT starts charging through the capacitances C_P and C_S. V_{gs_I}, V_{CP_I}, and V_{CS_I} voltages at the end of the period I are shown in equations (5), (6), and (7).

$$V_{gs_I} = V_F \tag{5}$$

$$V_{CP_I} = (V_S - V_F)\frac{C_S}{C_P + C_S} \tag{6}$$

$$V_{CS_I} = (V_S - V_F)\frac{C_P}{C_P + C_S} \tag{7}$$

TERM II [$T_1 \le t \le T_2$]:

When turn-on is completed at T_1, v_{gs} is clamped by the forward voltage (V_F) of the parasitic diode D_{gs}. The capacitances C_P and C_S are discharged and charged through the resistances R_P and R_S. V_{CP_II} and V_{CS_II} voltages at the end of the period II are expressed by equations (8) and (9) using the general equation[12] of MOSFET.

$$V_{CP_II} = V_{CP_I}\left(1 - \frac{C_P + C_S}{C_S}\frac{R_P}{R_P + R_S}\right)\cdot \exp\left[\frac{-(T_2 - T_1)}{\left(\frac{R_P \cdot R_S}{R_P + R_S}\right)(C_P + C_S)}\right] + (V_S - V_F)\frac{R_P}{R_P + R_S} \tag{8}$$

$$V_{CS_II} = V_{CS_I}\left(\frac{C_P + C_S}{C_P}\frac{R_S}{R_P + R_S} - 1\right)\left[1 - \exp\left[\frac{-(T_2 - T_1)}{\left(\frac{R_P \cdot R_S}{R_P + R_S}\right)(C_P + C_S)}\right]\right] + V_{CS_I} \tag{9}$$

TERM III [$T_2 \le t \le T_3$]:

When switch S2 is turned on at T_2, the capacitance C_{iss} of the GaN GIT starts charging through the capacitances C_P and C_S. When the electric charge of each capacitor is balanced, the discharge ends. V_{gs_III}, V_{CP_III}, V_{CS_III}, and V_{qs_III} voltages at the end of the period III are shown in equations (10) to (13). These are derived by applying charge conservation. In order to realize two-step turn-off, it is necessary to clamp V_{qs_III} at a value higher than the threshold voltage (V_{th}). As a result, the spike gate voltage is reduced in comparison with the conventional RC type circuit (Fig. 6).

$$V_{gs_III} = \frac{C_P\left[Q_g - V_{CS_II}\cdot C_S\right] + C_S\left[Q_g - V_{CP_II}\cdot C_P\right]}{\left(C_P\cdot C_S + C_S\cdot C_{iss} + C_{iss}\cdot C_P\right)} \tag{10}$$

$$V_{CP_III} = \frac{C_S\left[V_{CP_II}\cdot C_P - Q_g\right] + C_{iss}\left[V_{CP_II}\cdot C_P - V_{CS_II}\cdot C_S\right]}{\left(C_P\cdot C_S + C_S\cdot C_{iss} + C_{iss}\cdot C_P\right)} \tag{11}$$

$$V_{CS_III} = \frac{C_P\left[V_{CS_II}\cdot C_S - Q_g\right] + C_{iss}\left[V_{CS_II}\cdot C_S - V_{CP_II}\cdot C_P\right]}{\left(C_P\cdot C_S + C_S\cdot C_{iss} + C_{iss}\cdot C_P\right)} \tag{12}$$

$$V_{qs_III} = V_{gs_III} + V_{CS_III} \tag{13}$$

TERM IV [$T_3 \le t \le T_4$]:

The capacitances C_{iss}, C_P, and C_S are discharged through the resistances R_P and R_S.

TERM V [$T_4 \le t \le T_5$]:

When the voltage v_{qs} between the gate terminal and the gate power supply GND terminal is lower than the threshold voltage (V_{th}), the MOSFET Q_S is turned on. Simultaneously, the capacitances C_{iss}, C_P, and C_S are instantly discharged in the path of the MOSFET Q_S.

TERM VI [$T_5 \le t \le T_6$]:

The capacitances C_{iss} and C_S are discharged through the resistance R_S. The gate voltage v_{gs} approaches 0 V at the above RC time constant.

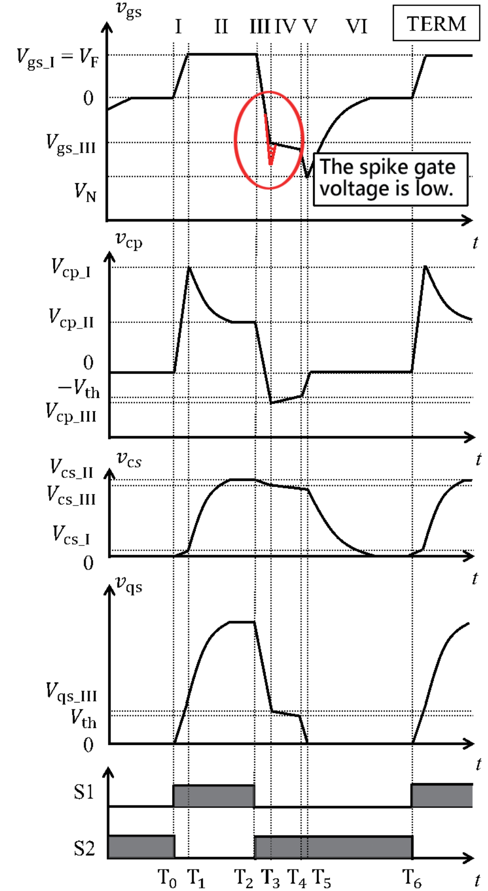


Fig. 6 Operation sequence of proposed gate drive circuit

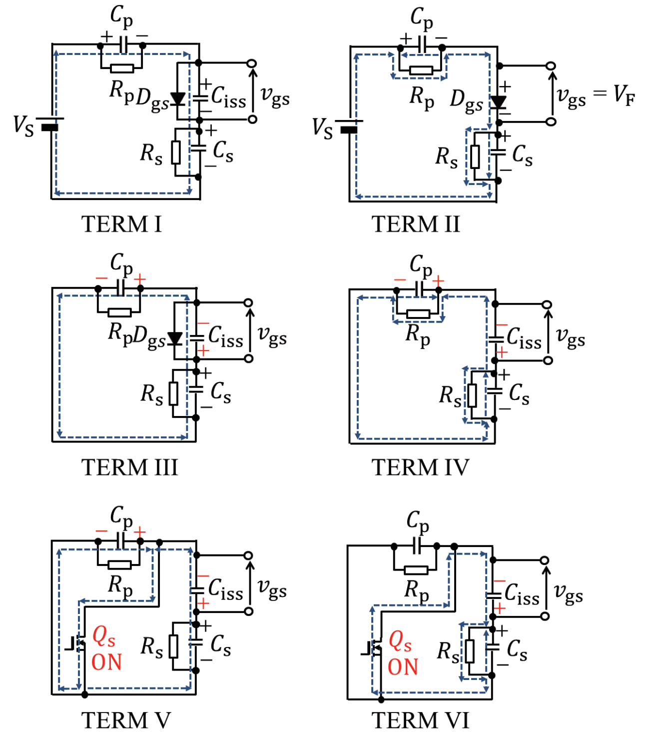


Fig. 7 Equivalent circuit of proposed gate drive circuit

4. Experiment results

Figs. 8 and 9 show the block diagram of the evaluation board used and the synchronous rectification type DC/DC converter. The conventional circuit and the proposed circuit were applied to the gate drive circuit (GD1 and GD2), and IGOT60R070D1 (Infineon)[13] was used as GaN GIT. Considering the rated operation region of the device, the evaluation was performed in the condition of the voltage boost operation of V_{in} = 150 V, V_{out} = 300 V, P_{out} = 0.25 − 1 kW, and f_{SW} = 20 kHz. Table 2 shows the parameters used. The capacitance C_P was adjusted at approximately V_N = −5.0 V in order to prevent incorrect turn-on of GaN GIT caused by the miller current.

Fig. 10 shows the result of the efficiency measurement. It is found that there is no difference in efficiency between the conventional circuit and the proposed circuit. Fig. 11 shows the waveform of the conventional gate drive circuit (Fig. 11 (a)) and the waveform of the proposed gate drive circuit (Fig. 11 (b)) in the condition of P_{out} = 1 kW. The left and right sides show the waveforms of turn-off of the devices Q_2 and Q_1, respectively. The voltage signals v_{gs} and v_{ds} were detected by the optical isolation differential probe (TIVM1 and TIVH08: manufactured by Tektronix Co.). The spike gate voltage at the turn-off of the device Q_1 is −12.8 V in the conventional circuit and −7.2 V in the proposed circuit. The spike gate voltage of the proposed circuit was improved by 5.6 V in comparison with the conventional one. Similarly, the spike gate voltage of the device Q_2 at the turn-off is −12.4 V in the conventional circuit and −4.0 V in the proposed circuit. The spike gate voltage of the proposed circuit was improved by 8.4 V in comparison with the conventional one. Since the proposed drive circuit can realize two-step turn-off switching at the turn-off of both devices Q_1 and Q_2, the generation of spike gate voltage is suppressed. Therefore, a sufficient margin can be secured for the rated gate-to-source voltage of −10 V. In addition, the switching speed of the drain-to-source voltage at the turn-off of Q_1 and Q_2 is not very different in comparison with the conventional circuit. Furthermore, in the proposed circuit, the miller noise that is superimposed onto the gate voltage during the switching period can be reduced, and it is considered that the low impedance of the gate circuit can be realized by the miller clamp MOSFET Q_S during the switching period. From these results, we were able to experimentally verify that the application of the two-step turn-off circuit allows the simultaneous satisfaction of the contrary performance of the low spike gate voltage and high speed turn-off switching.

Table 2 Evaluation condition

Components	Constant	
	Conventional circuit	Proposed circuit
R_p	330 Ω	130 Ω
R_s	—	200 Ω
R_{gon}	22 Ω	22 Ω
R_{goff}	0 Ω	0 Ω
C_p	3.2 nF	1.0 nF
C_s	—	22 nF

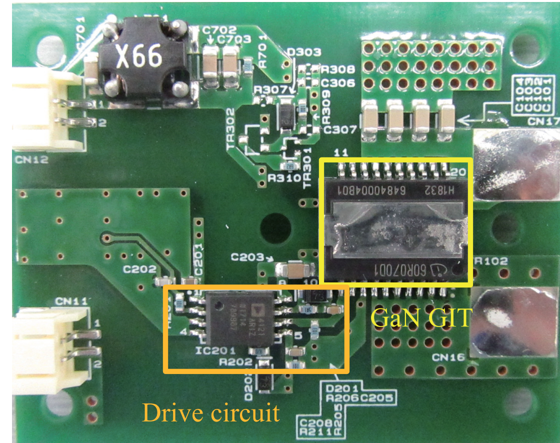


Fig. 8 Evaluation board

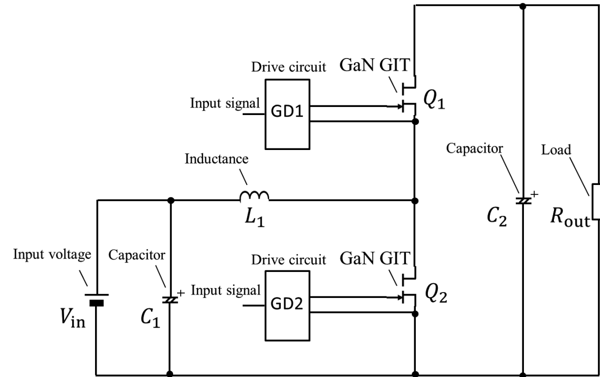


Fig. 9 Synchronous rectification type DC/DC converter

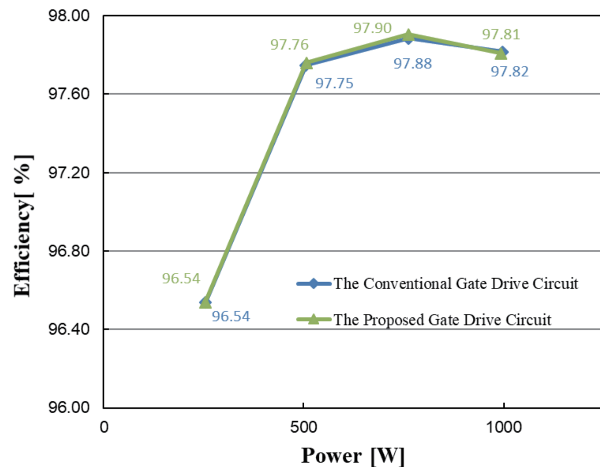
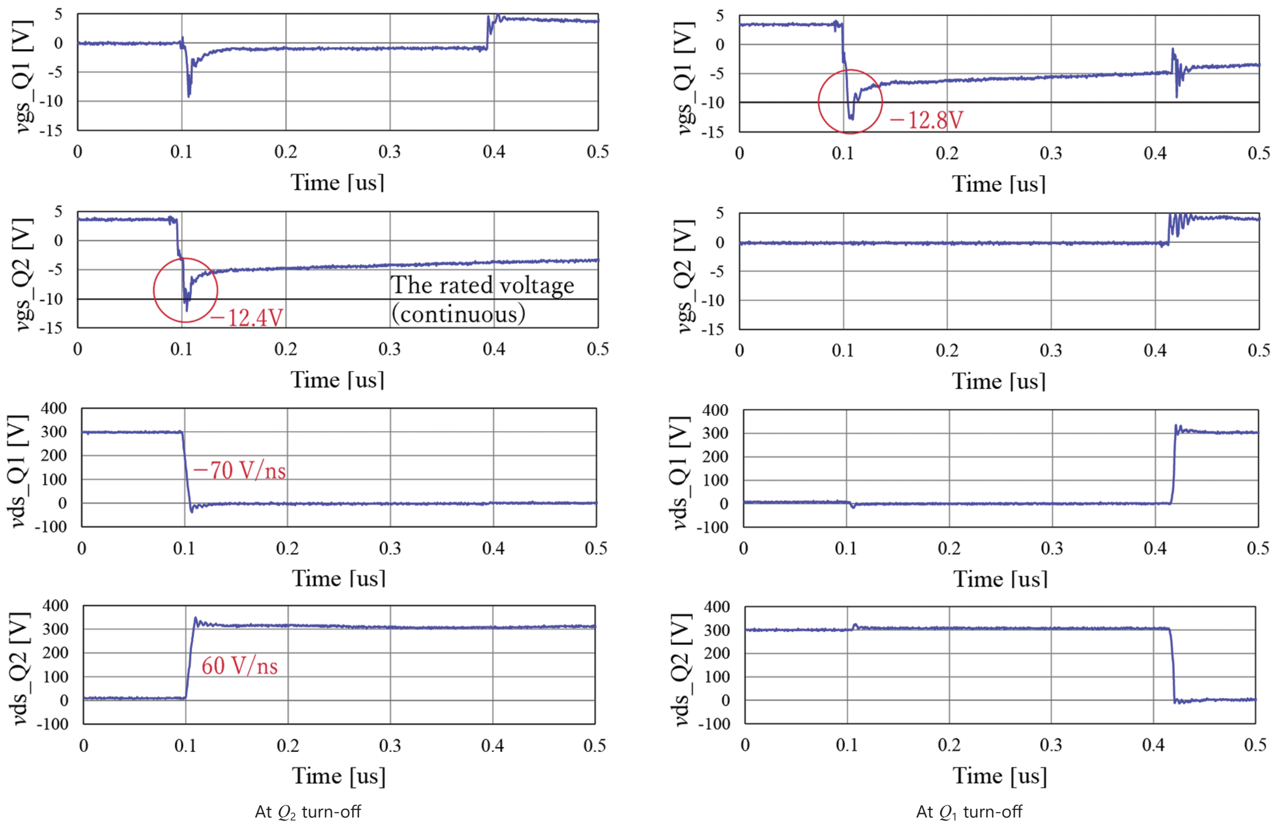
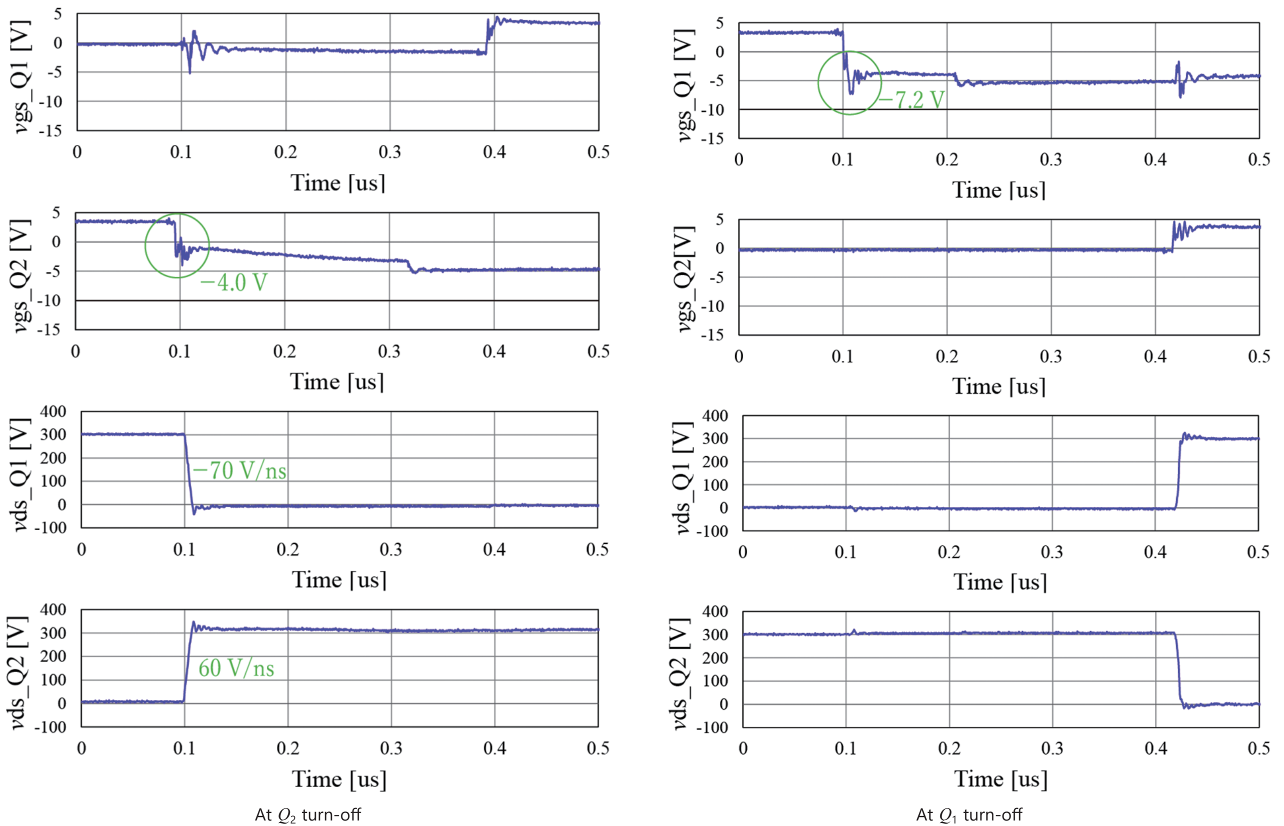


Fig. 10 Evaluation results of efficiency measurement



(a) Conventional gate drive circuit



(b) Proposed gate drive circuit

Fig. 11 Evaluation results of waveform measurement

5. Conclusions

The conventional gate drive circuit had the task that the high spike gate voltage generated at switching hinders high speed switching and higher efficiency. Therefore, this paper proposed the two-step turn-off method for the GaN GIT gate drive capable of simultaneously realizing the contrary performance of low noise and high speed turn-off switching. We mounted it to the synchronous rectification type DC/DC converter using the proposed gate drive circuit to evaluate the actual machine. We verified that the spike gate voltage was reduced by a maximum of 8.4 V without impairing the high speed turn-off switching characteristics and efficiency and showed the effectiveness of this system by securing the sufficient margin for the rated gate-to-source voltage of −10 V.

Hereafter we will study the optimization of the circuit constant matching the drive conditions.

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